programming a plurality of threshold voltages in a reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;

electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and

fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.

64. A method according to claim 63 further comprising the steps of:

sensing a voltage from an individual memory cell of the nonvolatile memory;

sensing a plurality of programmed threshold voltages from the reference storage;

comparing the sensed voltage from the individual memory cell to the sensed plurality of programmed threshold voltages from the reference storage; and

determining a multiple-bit data value based on the comparison result.

65. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of:

programming an individual electrically-erasable reference cell to define a plurality of data states in the individual memory cell of the nonvolatile memory.

66. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of:

programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

67. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of:

programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory; and

programming individual electrically-erasable reference cells of the plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

68. An electronic system including a processor, a memory and a system bus comprising:

a memory circuit performing the method according to claim 63.

69. A memory circuit for operating a nonvolatile memory comprising:

a reference storage;

means coupled to the reference storage for programming a plurality of threshold voltages in the reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;

means coupled to the reference storage for electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and

means coupled to the reference storage for fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.

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8 ~~70.~~ A memory circuit according to claim ~~69~~ 7 further comprising:

means for sensing a voltage from an individual memory cell of the nonvolatile memory;

means coupled to the reference storage for sensing a plurality of programmed threshold voltages from the reference storage;

means coupled to the reference storage and coupled to the nonvolatile memory for comparing the sensed voltage from the individual memory cell to the sensed plurality of programmed threshold voltages from the reference storage; and

means coupled to the comparing means for determining a multiple-bit data value based on the comparison result.

9 ~~71.~~ A memory circuit according to claim ~~69~~ 7 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises:

means for programming an individual electrically-erasable reference cell to define a plurality of data states in the individual memory cell of the nonvolatile memory.

10 ~~72.~~ A memory circuit according to claim ~~69~~ 7 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises:

means for programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

11 ~~73.~~ A memory circuit according to claim ~~69~~ 7 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises:

means for programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory; and

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